

**CONTENT ADDRESSABLE MEMORY (CAM) DEVICES  
HAVING ERROR DETECTION AND CORRECTION CONTROL  
CIRCUITS THEREIN AND METHODS OF OPERATING SAME**

Abstract of the Disclosure

Content addressable memory (CAM) devices include error detection and correction (EDC) control circuits therein. The EDC control circuit operates to correct soft errors in entries within a plurality of internal CAM array blocks with, at most, limited interruption to other operations performed by the CAM device. The EDC control circuit utilizes a multi-bit check word associated with each entry to detect a soft error and perform one-bit error correction on the entry. The EDC control circuit is configured to be active during a background mode of operation when the CAM array blocks are undergoing search operations in a foreground mode of operation. A CAM array block may also include a column of dual-function check bit cells that are configured to operate as a column of CAM cells when necessary to replace a defective column of CAM cells.

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